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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/769,956	01/25/2001	William J. Walker	COMP:0041/FLE(P00-2992)	5915

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INTELLECTUAL PROPERTY ADMINISTRATION
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EXAMINER	
LE, DIEU MINH T	
ART UNIT	**PAPER NUMBER**
2114	9

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/769,956	Applicant(s) WALKER ET AL.	
	Examiner Dieu-Minh Le	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-85 are again presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 43 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 43, line 2, claim "38" should be changed to -39- since claim 38 is memory sub-system not the system for correcting errors detected in a memory device as claimed in claim 43. Clarification is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-85 are rejected under 35 U.S.C. § 103(a) as being unpatentable Gonzales et al. (US Patent 6,101,614 hereafter referred to as Gonzales) in view of Arnold et al. (US Patent 6,279,128 hereafter referred to as Arnold).

As per claim 1:

Gonzales substantially teaches the invention. Gonzales teaches:

- a system for detecting errors in a memory device [abstract, fig. 3, col. 2, lines 35-40]comprising:
- a memory sub-system [fig. 3, col. 2, lines 37-40];
- a plurality of memory cartridges configured to stored data words ***(i.e., memory array via multiple memory configuration)*** [col. 3, lines 24-34 and col. 4, lines 31-39];
- a cleansing device configured to periodically initiate an internal READ command to plurality of memory cartridges in response to an event, the internal READ command being issued to plurality of memory cartridges on a memory network bus [col. 2, lines 58-68 and col. 7, lines 40-55];
- host controller (i.e., controller) coupled to the memory and comprising error detection logic configured to detect errors [col. 2, lines 58-60] from memory.

Gonzales does not explicitly teach:

- a monitoring device configured to monitoring the memory network bus and configured to change the frequency of periodic initiations of the internal READ command.

In addition, Arnold explicitly teaches:

- a system for continuous monitoring and detection of memory system [abstract, fig. 1, col. 9, lines 36-42]comprising:
- plurality of DRAM memory array (i.e., memory modules) with controller connected to ECC, scrub sequencer, address controller, etc... [fig. 2, col. 5, lines 12-26];
- a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer [col. 6, lines 6-53].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made; first, to realize the Gonzales 's method and apparatus for automatically scrubbing ECC errors in memory comprising a connectivity among memory array, memory controller, memory interface controller, processors, I/O user interfaces, via network bus and more specifically the memory module buffers control logic, memory address control logic, memory controller,

a central control logic used to calculate parity data as well as to initiate READ commands for configuring networking bus as being the monitoring device configured to monitoring the memory network bus and configured to change the frequency of periodic initiations of the internal READ command as claimed by Applicant. This is because the Gonzales' method and apparatus for automatically scrubbing ECC errors in memory does perform the memory access control functionality to ensuring error detected and corrected properly within the memory device via a control logics that establishes and initiates the operational commands such as READ, WRITE requests, etc.... in supporting the memory error detection and correction. It is further obvious to an ordinary skill in the art to understand the Gonzales's control logic does perform the programming or configuring (i.e., monitoring) its capability to add, distribute, and calculate the parity data in the memory modules; second, one would modify the Gonzales's computer system to explicitly including the a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer as taught by Arnold's system for continuous monitoring and detection of memory system in supporting data transmission/processing within memory data modules via control logic capability.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the memory system with plurality of memory modules or memory arrays and more specifically to a RAID array memory with a mechanism to enhance data performance/monitoring, data availability/reliability, and data configuring/exchanging operation via EEC means for data recovery process. It is further obvious because by utilizing this approach, memory system with a processor-based computer can be realized in high performance throughput with a high reliability and flexibility memory environment.

As per claims 2-6:

Gonzales substantially teaches the invention. Gonzales teaches:

- a system for detecting errors in a memory device [abstract, fig. 2 and 3, col. 1, lines 11-15]comprising:
- a plurality of memory cartridges configured to stored data words ***(i.e., memory array via multiple memory configuration)*** [col. 3, lines 24-34 and col. 4, lines 31-39];
- memory modules comprising a Dual Inline Memory Module ***(i.e., double and single sided SIMM)*** [col. 4, lines 40-52];

- memory and comprising error detection logic configured to detect errors [col. 3, lines 42-50, col. 3, lines 66 through col. 4, lines 12];

- a memory controller operably coupled to the memory sub-system and configured to control access to memory [fig. 2 and 3, col. 4, lines 19-23].

Gonzales does not explicitly teach:

- a Synchronous Dynamic Random Access Memory (SDRAM) device.

However Gonzales does disclose capability of:

- a method and apparatus for automatically scrubbing ECC errors in memory [abstract, fig. 2 and 3, col. 1, lines 11-15] comprising:

- a connectivity among memory array, memory controller, memory interface controller, processors, I/O user interfaces, hard drive, and other computing devices [fig. 1-3, col. 4, lines 14 through col. 5, lines 36];

- a memory controller capability to orchestrate data transferring, data control, effectively access DRAM array [col. 5, lines 1-55];

In addition, Arnold explicitly teaches:

- a system for continuous monitoring and detection of memory system [abstract, fig. 1, col. 9, lines 36-42]comprising:
- plurality of DRAM memory array (i.e., memory modules) with controller connected to ECC, scrub sequencer, address controller, etc... [fig. 2, col. 5, lines 12-26];

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize the Gonzales' method and apparatus for automatically scrubbing ECC errors in memory including plurality of DRAM memory array do embedded the Synchronous Dynamic Random Access Memory (SDRAM) device as indicated by Applicant. This is because the SDRAM memory device is part of RAID, SIMM, and DIMM families of memory. Therefore, it would have been obvious to an ordinary skill in the art to readily use and apply the SDRAM memory device within the error detection and correction environment.

As per claims 7-12:
Gonzales substantially teaches the invention. Gonzales teaches:
- a system for detecting errors in a memory device [abstract, fig. 2 and 3, col. 1, lines 11-15]comprising:

- a plurality of memory cartridges configured to stored data words ***(i.e., memory array via multiple memory configuration)*** [col. 3, lines 24-34 and col. 4, lines 31-39];
- a memory sub-system [fig. 3, col. 2, lines 37-40];
- a cleansing device configured to periodically initiate an internal READ command to plurality of memory cartridges in response to an event, the internal READ command being issued to plurality of memory cartridges on a memory network bus [col. 2, lines 58-68 and col. 7, lines 40-55];
- memory module control logic, memory address control logic, memory controller, a central control logic used to calculate parity data as well as to initiate READ commands for configuring networking bus [fig. 3, col. 2, lines 58-60];
- a data/error code correction (ECC) used error detection and correction [col. 3, lines 14-18].

In addition, Arnold explicitly teaches:
- a system for continuous monitoring and detection of memory system [abstract, fig. 1, col. 9, lines 36-42] comprising:
- a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer [col. 6, lines 6-53].

- the event comprising an operator instruction (i.e., code signature) [abstract, col. 4, lines 10-21].

As per claims 13-20:

Gonzales substantially teaches the invention. Gonzales teaches:

- a system for detecting errors in a memory device [abstract, fig. 2 and 3, col. 1, lines 11-15]comprising:
- a memory sub-system [fig. 3, col. 2, lines 37-40];
- a plurality of memory cartridges configured to stored data words ***(i.e., memory array via multiple memory configuration)*** [col. 3, lines 24-34 and col. 4, lines 31-39];
- a cleansing device configured to periodically initiate an internal READ command to plurality of memory cartridges in response to an event, the internal READ command being issued to plurality of memory cartridges on a memory network bus [col. 2, lines 58-68 and col. 7, lines 40-55];
- host controller (i.e., controller) coupled to the memory and comprising error detection logic configured to detect errors [col. 2, lines 58-60] from memory.

Gonzales does not explicitly teach:

- a monitoring device configured to monitoring the memory network bus and configured to change the frequency of periodic initiations of the internal READ command.

In addition, Arnold explicitly teaches:

- a system for continuous monitoring and detection of memory system [abstract, fig. 1, col. 9, lines 36-42]comprising:
- plurality of DRAM memory array (i.e., memory modules) with controller connected to ECC, scrub sequencer, address controller, etc... [fig. 2, col. 5, lines 12-26];
- a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer [col. 6, lines 6-53].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made; first, to realize the Gonzales 's method and apparatus for automatically scrubbing ECC errors in memory comprising a connectivity among memory array, memory controller, memory interface controller, processors, I/O user interfaces, via network bus and more specifically the memory module buffers control logic, memory address control logic, memory controller, a central control logic used to calculate parity data as well as

to initiate READ commands for configuring networking bus as being the monitoring device configured to monitoring the memory network bus and configured to change the frequency of periodic initiations of the internal READ command as claimed by Applicant. This is because the Gonzales' method and apparatus for automatically scrubbing ECC errors in memory does perform the memory access control functionality to ensuring error detected and corrected properly within the memory device via a control logics that establishes and initiates the operational commands such as READ, WRITE requests, etc.... in supporting the memory error detection and correction. It is further obvious to an ordinary skill in the art to understand the Gonzales's control logic does perform the programming or configuring (i.e., monitoring) its capability to add, distribute, and calculate the parity data in the memory modules; second, one would modify the Gonzales's computer system to explicitly including the a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer as taught by Arnold's system for continuous monitoring and detection of memory system in supporting data transmission/processing within memory data modules via control logic capability.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the memory system with plurality of memory modules or memory arrays and more specifically to a RAID array memory with a mechanism to enhance data performance/monitoring, data availability/reliability, and data configuring/exchanging operation via EEC means for data recovery process. It is further obvious because by utilizing this approach, memory system with a processor-based computer can be realized in high performance throughput with a high reliability and flexibility memory environment.

As per claims 21-38, 43:

Due to the similarity of claims 21-38 to claims 1-20 except for a memory sub-system comprising capabilities of plurality of memory cartridge, a cleansing device, a monitoring device, etc... instead of a system for detecting errors in a memory device including a memory sub-system comprising capabilities of plurality of memory cartridge, a cleansing device, a monitoring device, etc...Therefore, theses claims are also rejected under the same rationale applied against claims 1-20. In addition, all of the limitations have been noted in the rejection as per claims 1-20.

As per claims 39-42, 44-66:

These claims are similar to claims 1-20. The only minor different is these claims introduce:

- a memory engine configured to correct the error detected in data word;
- scrubbing control logic configured to request a write-back to memory;
- a content addressable memory (CAM).

However, Gonzales teaches:

- a system for detecting errors in a memory device [abstract, fig. 3, col. 2, lines 35-40]comprising:
- a memory sub-system [fig. 3, col. 2, lines 37-40];
- a plurality of memory cartridges configured to stored data words ***(i.e., memory array via multiple memory configuration)*** [col. 3, lines 24-34 and col. 4, lines 31-39];
- a cleansing device configured to periodically initiate an internal READ/WRITE command to plurality of memory cartridges in response to an event, the internal READ/WRITE command being issued to plurality of memory cartridges on a memory network bus [col. 2, lines 58-68 and col. 7, lines 40-55];
- host controller (i.e., controller) coupled to the memory and comprising error detection logic configured to detect errors [-memory module control logic, memory address control logic (i.e.,

CAM), memory controller, a central control logic used to calculate parity data as well as to initiate READ commands for configuring networking bus [col. 2, lines 58-60];

- a data/error code correction (ECC) used error detection and correction [abstract, col. 3, lines 14-18].

In addition, Arnold explicitly teaches:

- a system for continuous monitoring and detection of memory system [abstract, fig. 1, col. 9, lines 36-42]comprising:

- plurality memory array with controller connected to ECC, scrub sequencer, address controller, etc... [fig. 2, col. 5, lines 12-26];

- a scrubbing means used to read/write data [col. 9, lines 35-48];

- a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer [col. 6, lines 6-53].

Therefore, these claims are also rejected under the same rationale applied against claims 1-20. In addition, all of the limitations have been noted in the rejection as per claims 1-20.

As per claims 67-85:

Firstly, due to the similarity of claims 67-85 to claims 1-20 except for a method for dynamically scheduling access to a memory steps including monitoring activity on a memory step, periodically initiating internal READ commands step, etc... instead of instead of a system for detecting errors in a memory device including a memory sub-system comprising capabilities of plurality of memory cartridge, a cleansing device configured to periodically initiating internal READ commands, a monitoring device, etc...Therefore, theses claims are also rejected under the same rationale applied against claims 1-20. In addition, all of the limitations have been noted in the rejection as per claims 1-20.

Secondly, a compared a threshold, RAID memory are also introduced in dependent claims 72,73, 84, and 85.
However, Arnold explicitly teaches:
- a system for continuous monitoring and detection of memory system [abstract, fig. 1, col. 9, lines 36-42];
comprising:
- plurality memory array with controller connected to ECC, scrub sequencer, address controller, etc... [fig. 2, col. 5, lines 12-26];
- a scrubbing means used to read/write data [col. 9, lines 35-48];

- a monitoring capability to performing and configuring READ commands based on network bus request, memory process, as well as scrub sequencer [col. 6, lines 6-53].

- a compared a threshold in supporting the error detection and correction system [col. 7, lines 23-43]

Therefore, these claims are also rejected under the same rationale applied against claims 1-20. In addition, all of the limitations have been noted in the rejection as per claims 1-20.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703) 305-9408. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel, can be reached on (703)305-9713. The fax phone number for this Group is (703)746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

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Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
3/17/04